**HO CHI MINH UNIVERSITY OF TECHNOLOGY**

**OFFICE FOR INTERNATIONAL STUDY PROGRAMS - OISP**

**Logic Design with HDL**

EXPERIMENT

**Combinational Logic Circuit**

**Group information:**

| Class : Logic Design with HDL (Lab)  Group : 2 | Lecturer’s comment |
| --- | --- |
| Full name:   1. Nguyễn Văn Bình : 2153223 2. Lê Minh Quý : 2153758 3. Trần Hải Đăng : 2153297 4. Phạm Đức Trung : 2153928 |  |

**1 Introduction**

**1.1 Aims**

• Practice in designing sequential logic circuits using Verilog HDL behavioral model.

• Understand the blocking/non-blocking assignment to design a combinational/sequential circuit.

• Understand finite state machine models and practice in model FSMs using Verilog HDL.

**1.2 Preparation**

• Read the laboratory materials before class.

• Review chapter 5-6 about Behavioral Model and Finite State Machine.

• Each group prepares at least one laptop with Vivado software installed.

**1.3 Report Requirements**

• Lab exercises will be reviewed directly in class.

• Write report (with circuit/simulation screenshots inserted) in pdf.

• Must have group ID, group member’s names and student IDs in the report.

• Compress the report with code files (only .v files) in only one .zip file, name the .zip the group ID (for example: Group 1.zip).

• Submit on BK-elearning by deadline.

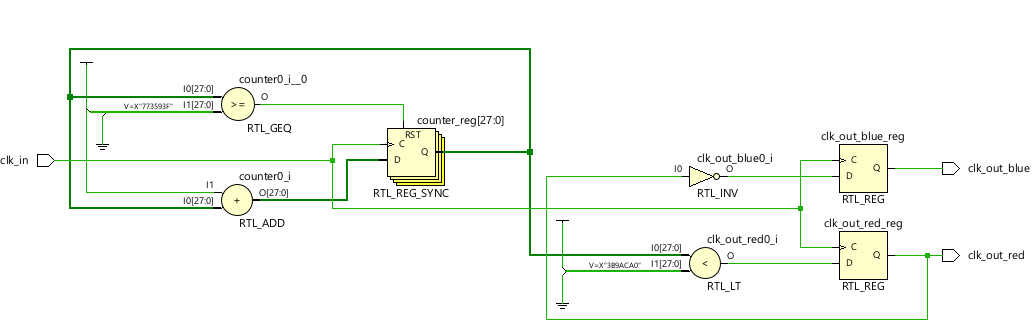
**2 Exercises**

**2.1 Exercises 1**

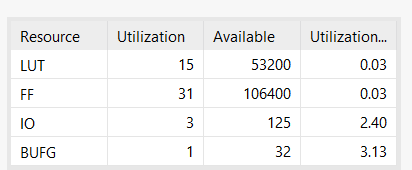
1. Police Siren

- Name of source files : policeSiren.v, siren\_tb.v

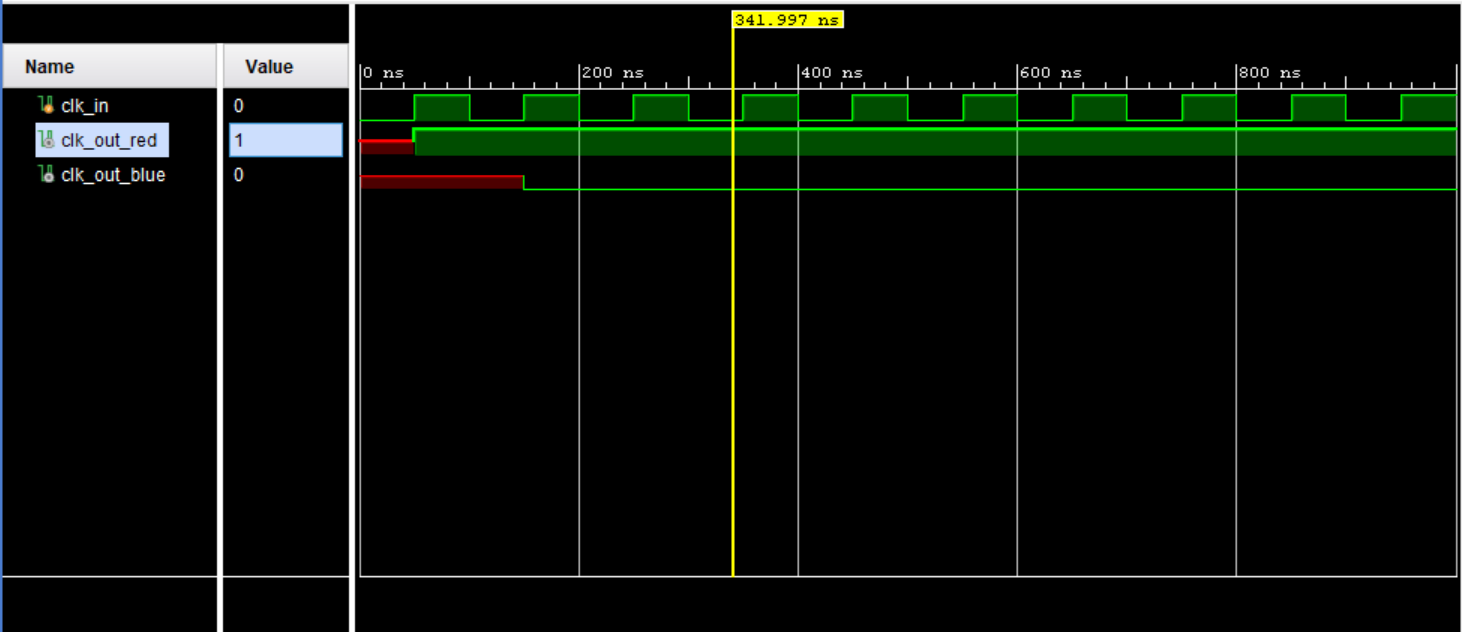
- RTL Schematic



-Resource Utilization



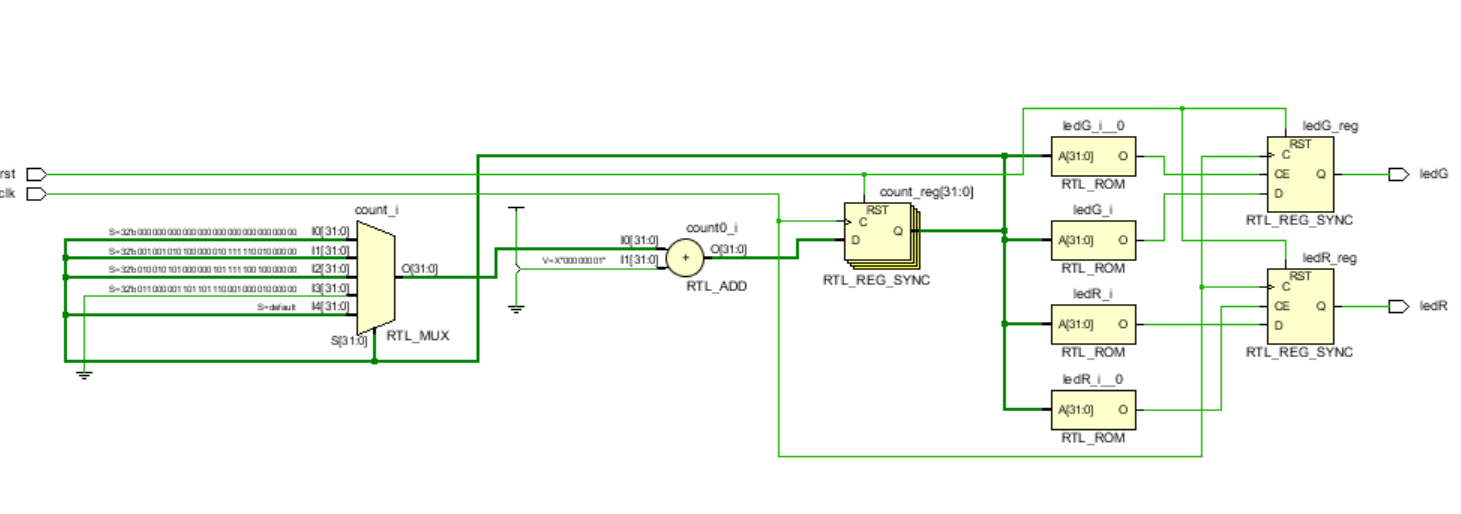
- Waveform



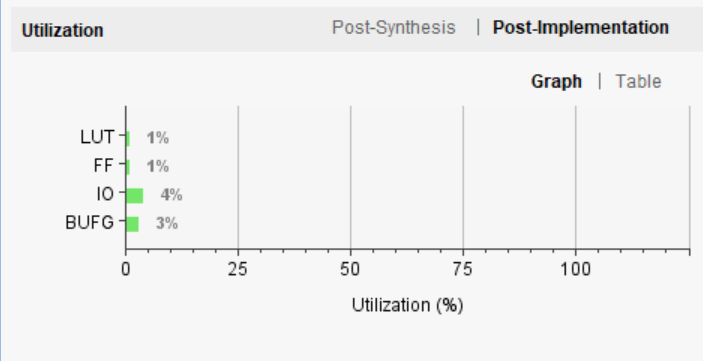
1. Crossroad traffic light

- Source files : ex1\_b.v, ex1\_b\_test

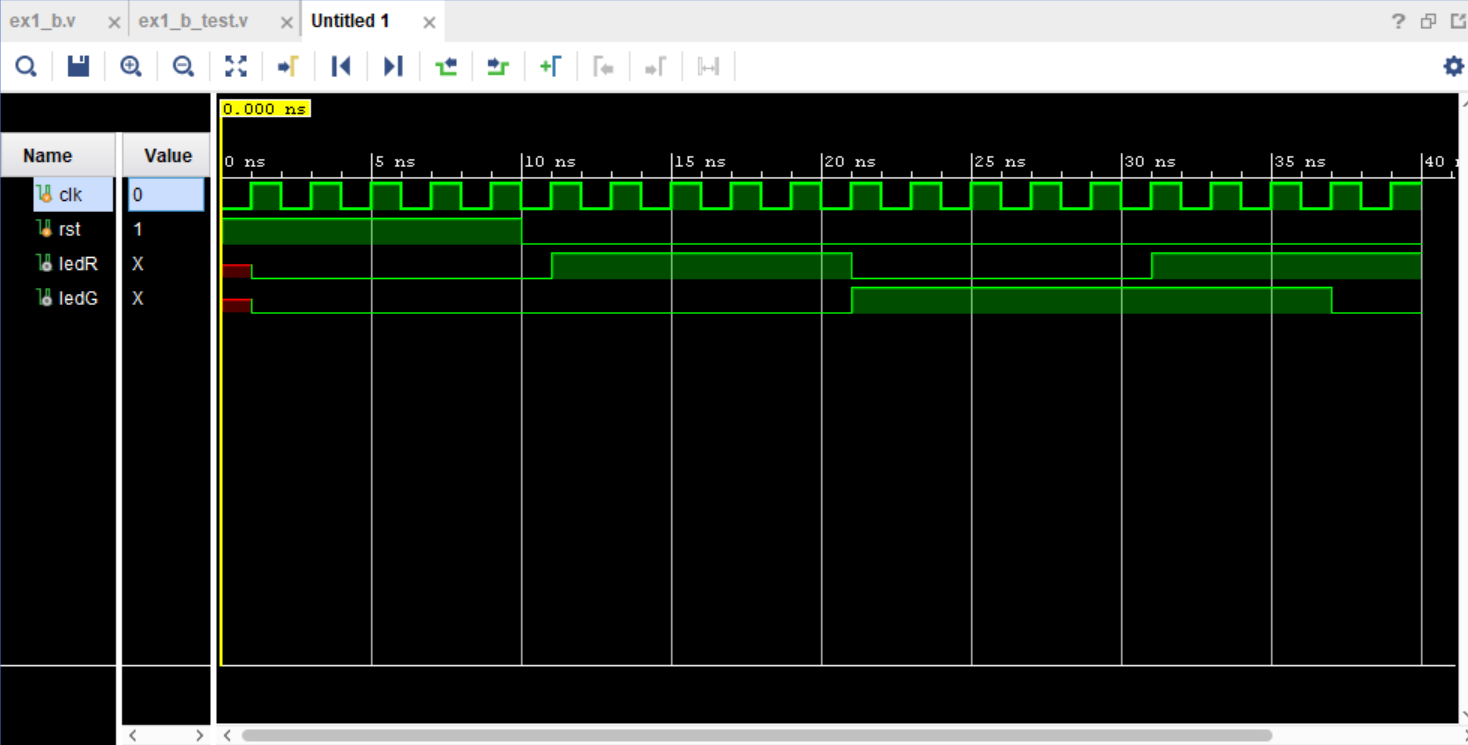
- RTL Schematic



- Utilization



- Waveform

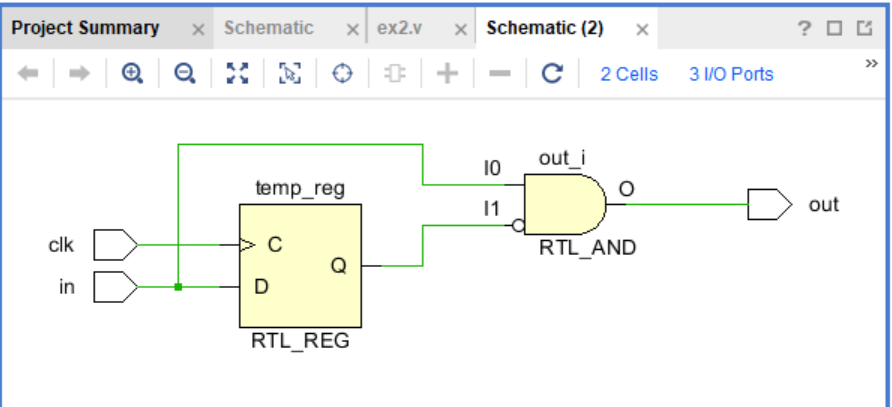


**2.2 Exercises 2**

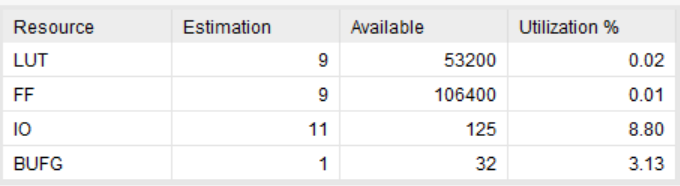
1. Edge Detection Circuit

- Source files : ex2.v, ex2\_tb.v

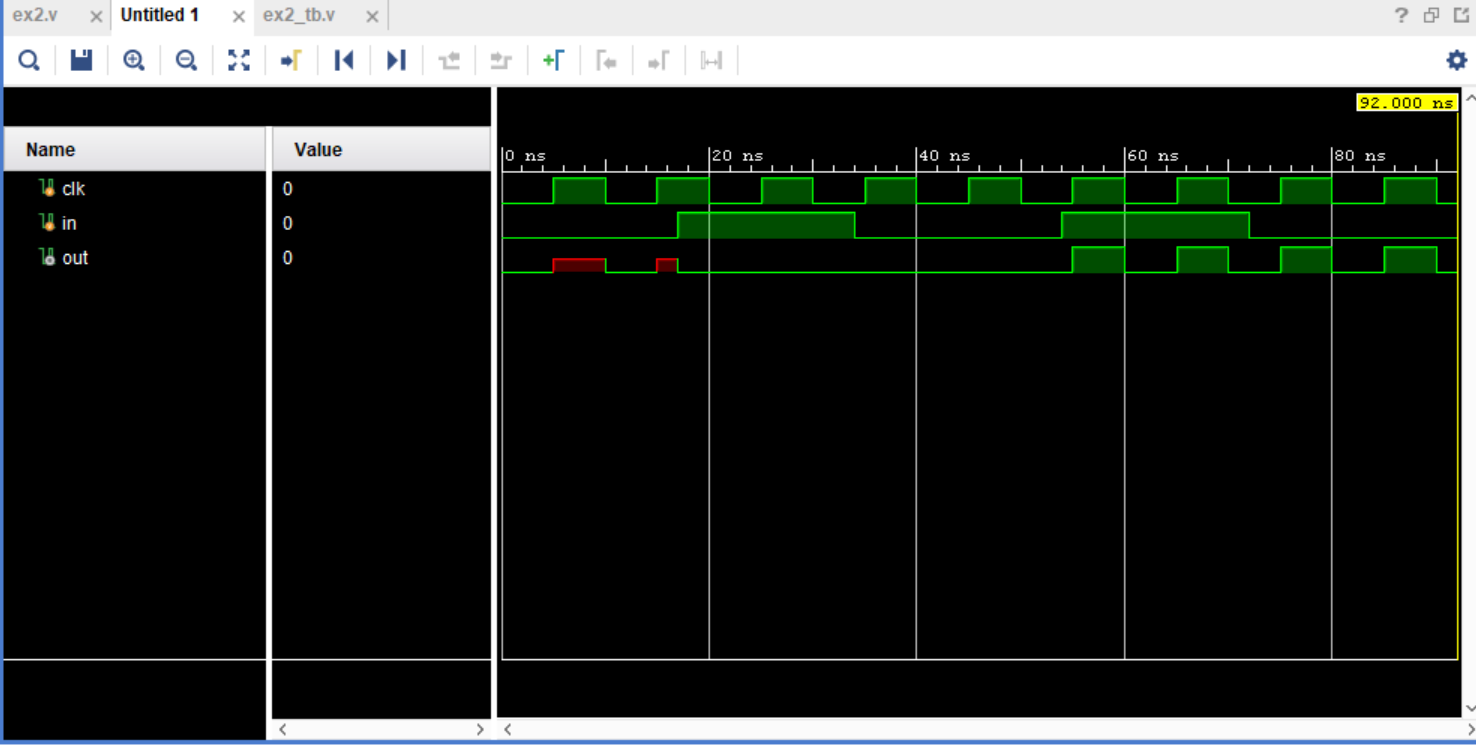
- RTL Schematic:



- Utilization

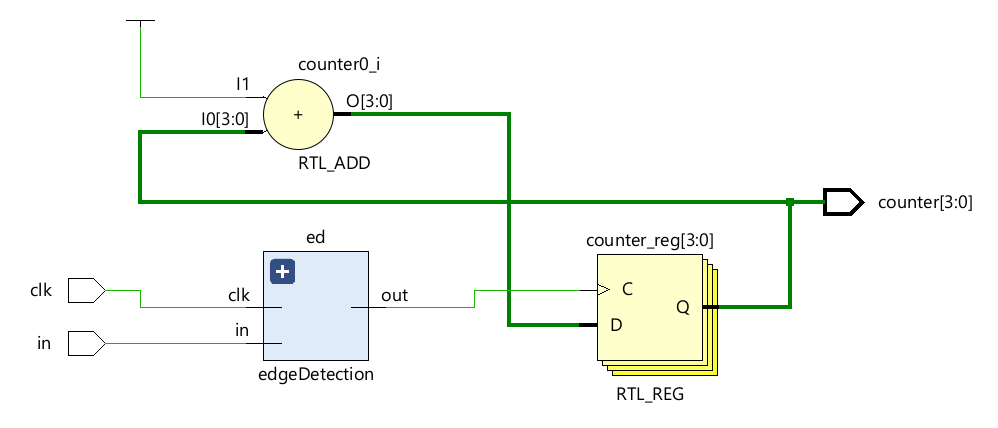


- Waveform

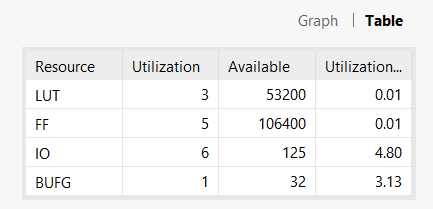


1. 4-bit binary counter

- Source Files : 4bit\_counter.v, edgeDetection.v

- RTL Schematic :

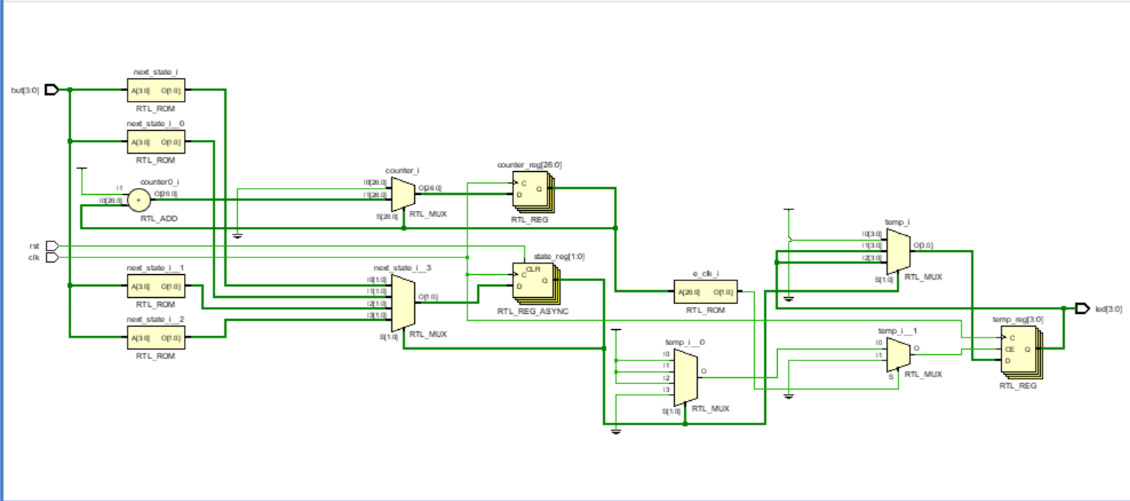
- Utilization :



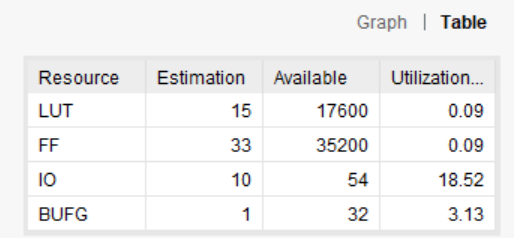
**2.3 Exercises 3**

-Source files : string\_led.v, shift\_led.tb.v

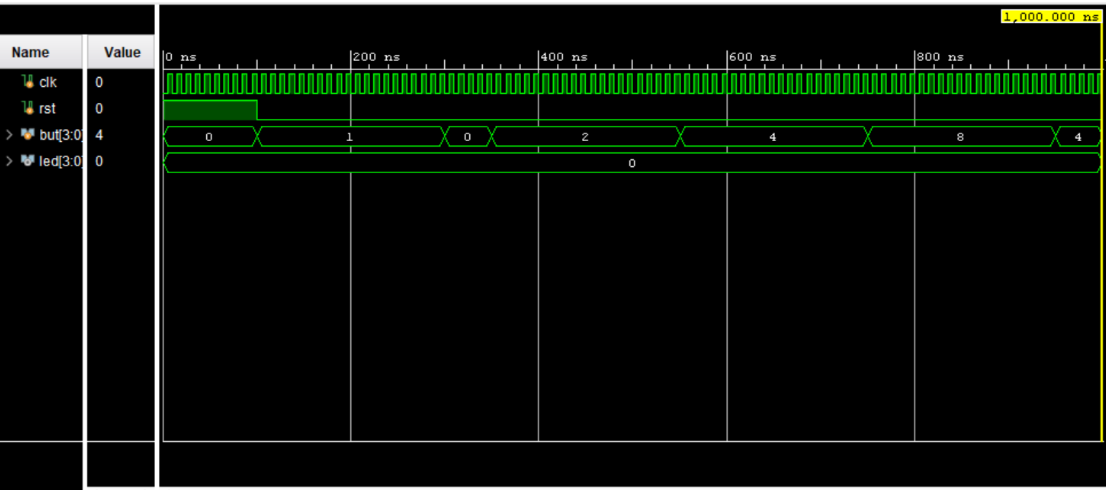
-RTL Schematic :



-Utilization



-Waveform



**End.**